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# A Low Capacitance Single-Phase AC-DC Converter with Inherent Power Ripple Decoupling

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**Abstract**—This paper proposes a new single-phase AC-DC conversion topology with inherent power ripple decoupling, based on the combination of a PWM H-bridge inverter, an AC side LC filter and a ZVS line commutated H-bridge. A capacitor on the AC side is used as power decoupling element. By appropriate selection of the capacitor voltage, the power ripple at twice the AC frequency can be cancelled from the DC side instantaneous power, achieving negligible DC voltage ripple using a smaller total capacitance compared to traditional solutions.

Recently, several solutions using the concept of Ripple-Port have been proposed that reduce the overall capacitance. However, they usually need at least a dedicated PWM half-bridge leg, adding switching loss, and a separate LC tank. Instead, the proposed topology integrates the ripple compensation in the AC/DC conversion stage, exploiting the AC filter and minimising additional loss thanks to the ZVS of the additional H-bridge.

The concept of the steady state operation of the proposed converter is described analytically and validated in simulation using MATLAB Simulink and PLECS.

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## I. INTRODUCTION

The diffusion of distributed generation and energy storage solutions is resulting in a growing need for single-phase AC-DC converters capable of unidirectional or bidirectional power flow, with rated powers often exceeding 1kW. Consequentially, a growing interest is arising in trying to develop more compact, efficient, reliable and inexpensive power converters that match those specifications. These converters can be generally intended for grid-connected or standalone applications.

One of the biggest problems of traditional single-phase power converters is the DC-link voltage ripple, caused by the oscillating nature at twice the AC frequency of single-phase instantaneous power. The power ripple requires the presence in the converter of a energy storage device in order to obtain power decoupling, i.e. to provide the power ripple at twice the AC frequency with negligible impact on the DC voltage.

The simplest and most common solution for this problem is to use a DC-link capacitor. This involves very high capacitance to contain voltage ripple, thus limiting the choice to electrolytic capacitors, that degrade reliability [1]. A large capacitor is needed because most of the energy stored in the DC-link capacitor does not contribute to power decoupling.

Many different approaches have been made in order to overcome this problem [2][3][4][5][6]. A comprehensive re-

view of those solutions is found in [7]. All those solutions make use of additional switches in order to control the power flowing in one or more power decoupling elements, usually grouped in a Ripple-Port, a dedicated section of the converter which is only used to provide the ripple power component. The presence of additional components for the Ripple-Port is essential in order to reduce the overall capacitance but it also involves higher costs, losses and reliability issues related to higher part count. In fact, operating a converter at unity power factor and injecting an active power  $P$ , the average of the absolute value of the power processed by the port is  $\frac{2}{\pi}P$ . This is processed by the power decoupling elements, and the following equation introduced in [4] can be used as an approximated evaluation of the impact of the Ripple-Port on the total conversion efficiency:

$$\eta = \eta_{main} - \frac{2}{\pi}(1 - \eta_{buffer}) \quad (1)$$

where  $\eta_{main}$  is the efficiency of the main inverter/rectifier and  $\eta_{buffer}$  is the efficiency of the additional section that provides power decoupling.

In [5] Caceres and Barbi proposed a power converter capable of power decoupling without using additional switches. A slightly different topology that exploits the same power-decoupling concept was introduced by Vasquez *et.al.* in [6]. The basic idea is that ripple power decoupling can be achieved integrating the Ripple-Port in the converter exploiting the LC output filter, rather than providing it with a dedicated circuit. This will minimise the need for additional components and their impact on efficiency and cost, while reducing the total capacitance. However, the capacitance needed tends to be higher than Ripple-Port based solutions.

This paper proposes a new topology built on the original concept proposed in [6] but completing it with a ZVS line-commutate H-bridge on the AC side, that can further reduce the converter capacitance with a limited increase in the complexity. The outcome is that values of total capacitance that are competitive with Ripple-Port solutions can be achieved with an integrated approach where no additional PWM legs are needed and the impact on the efficiency of the converter can be minimised.

The paper includes detailed analysis of the steady state waveforms of the proposed topology, together with a sizing

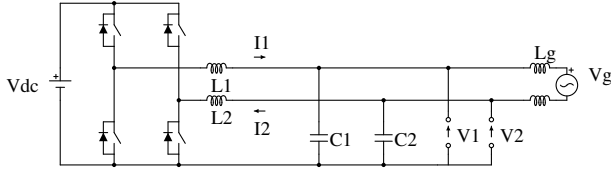


Fig. 1. Dual DC-DC [6]

procedure for the AC side capacitor used for power decoupling. The design has been validated in a closed loop time domain simulation and compared with Ripple-Port solutions, showing promising performances.

## II. POWER DECOUPLING

The energy balance of a converter can be expressed as in eq.2, where  $E(t)$  it the function of energy stored in the converter over time,  $t_0$  is an arbitrary instant of time, and  $P_{in}$ ,  $P_{out}$  are the power flowing in and out of the converter.

$$E(t) - E(t_0) = \int_{t_0}^t P_{in}(t^*) - P_{out}(t^*) dt^* \quad (2)$$

Assuming the power transferred from the DC source to the grid to be constant and equal to  $P$ , i.e. ideal power decoupling is in place, the inverter to operate at unitary power factor and neglecting losses, the difference between the instantaneous powers flowing in and out the inverter is calculated as follows:

$$V_g(t) = \sqrt{2}V_g \sin(\omega t) \quad I_g(t) = \sqrt{2}\frac{P}{V_g} \sin(\omega t) \quad (3)$$

$$P_{out} = V_g(t) I_g(t) = P [1 - \cos(2\omega t)] \quad P_{in} = P \quad (4)$$

$$P_{in}(t) - P_{out}(t) = P \cos(2\omega t) \quad (5)$$

Where  $V_g$  is the RMS line voltage and  $\omega$  is line pulsation.

Substituting in 2, the result is:

$$E(t) - E(t_0) = \int_{t_0}^t P \cos(2\omega t^*) dt^* \quad (6)$$

Energy stored in the reactive elements is a function of the voltages in capacitors and current in inductors. For simplicity, the converter is assumed to be designed such that the energy stored in inductors and in small size filter capacitors is negligible, so that only few power ripple decoupling capacitors are taken into account in the power balance.

$$E(t) = \frac{1}{2} \sum_i C_i V_i^2(t) \quad (7)$$

Substituting 7 in 6 results is a relation between voltages in power decoupling capacitors over time, valid for all the topologies with capacitive decoupling.

$$\frac{1}{2} \sum_i C_i [V_i^2(t) - V_i^2(t_0)] = \int_{t_0}^t P \cos(2\omega t^*) dt^* \quad (8)$$

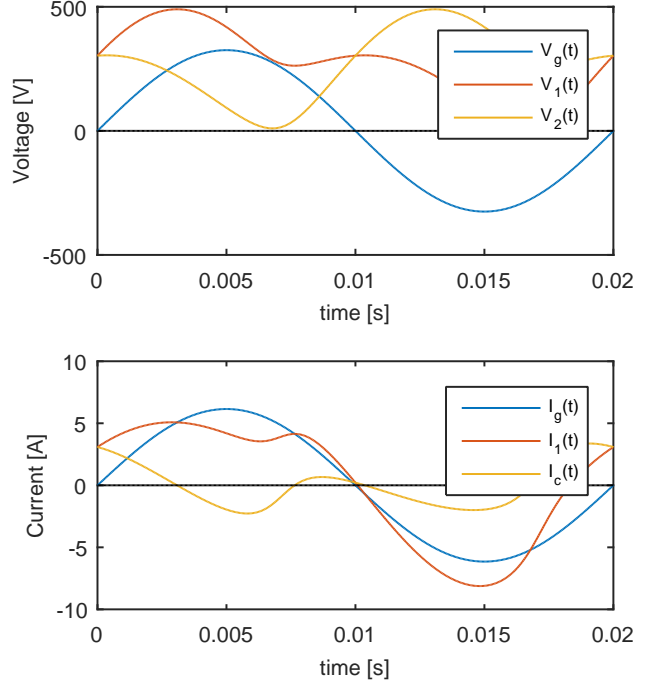


Fig. 2. Voltage and current waveforms  
 $V_{DC} = 500V$ ,  $P = 1kW$ ,  $C_1 = C_2 = 28\mu F$

## III. INHERENT RIPPLE POWER DECOUPLING CONCEPT

In [5] Caceres and Barbi proposed a new type of DC-AC converter, composed of two independent DC-DC Boost converters. Vasquez *et. al.* extended the same concept to Buck and Buck-boost converters[6], as shown in figure 1 for the Buck topology. Despite their simple structure, those DC-AC converters based on the dual connection of DC-DC converters provide significant advantages:

- Power ripple decoupling exploiting the AC capacitors, achieved controlling the common mode voltage generated by the two converters, without a bulky DC-link capacitor and without additional switches;
- The same capacitors used as energy storage for power decoupling also work as filters.

Being the two arms of the converter identical, they are modulated so that each of them produces an output voltage referred to the negative of the DC link which is a line frequency sinusoid at the grid frequency with half the desired grid voltage amplitude, added to a common mode voltage used to control the instantaneous power flowing in  $C_1$  and  $C_2$ . The two sinusoidal components at the grid frequency are in phase opposition, so that the difference between the two output voltages is equal to the desired voltage on the grid side.

In [6], the operation of the power ripple decoupling is forced by the control system, but a justification of the steady state waveforms is not provided analytically. This is provided

in the next subsection, and will be extended later with the introduction of the new proposed topology.

1) *Analysis of the capacitors voltages under ideal power ripple compensation:* In order to calculate the desired steady-state value of voltages in capacitors  $V_1$  and  $V_2$ , equation 8 can be used. Since the unknown functions are two another constraint is needed, which is that the differential voltage must be equal to line voltage.

$$V_1(t) - V_2(t) = V_g(t) = \sqrt{2}V_g \sin(\omega t) \quad (9)$$

The voltages at time  $t = t_0$  must be known too. Choosing  $t_0 = 0$  simplifies the problem, since at  $t = 0$  grid voltage is zero (according to 3) and so  $V_1(0) = V_2(0)$ . The resulting voltages are:

$$V_1(t) = \sqrt{\frac{P}{2\omega C} \sin(2\omega t) - \frac{V_g^2}{2} \sin(\omega t)^2 + V_0^2} + \frac{V_g \sin(\omega t)}{\sqrt{2}} \quad (10)$$

$$V_2(t) = \sqrt{\frac{P}{2\omega C} \sin(2\omega t) - \frac{V_g^2}{2} \sin(\omega t)^2 + V_0^2} - \frac{V_g \sin(\omega t)}{\sqrt{2}} \quad (11)$$

Where  $C_1 = C_2 = C$  and  $V_1(0) = V_2(0) = V_0$ .

Since all ripple power is compensated by  $C_1$  and  $C_2$ , ideally no voltage ripple is present on the DC link, with exception for PWM frequency ripple. Since the waveforms of voltages  $V_1$  and  $V_2$  are a function of  $V_0$  and  $C$  for a given power level and a given grid voltage, particular attention must be paid in the choice of  $C$  and  $V_0$  in order to provide power decoupling while respecting the constraints of minimum and maximum voltage that can be generated by the PWM bridge. In particular,  $V_0$  is an important degree of freedom, because it can be selected to respect the constants, at the same time trying to use the minimum value for the decoupling capacitors  $C$ .

2) *Analysis of the converter currents under ideal power ripple compensation:* The currents flowing in each capacitor  $I_{C1}(t)$  and  $I_{C2}(t)$  are calculated knowing their voltage over time, and the currents flowing in each arm of the bridge  $I_1(t)$  and  $I_2(t)$  as sum of the capacitor current and grid current.

$$I_{C1}(t) = C \frac{d}{dt} V_1(t) \quad I_{C2}(t) = C \frac{d}{dt} V_2(t) \quad (12)$$

$$I_1(t) = I_{C1}(t) + I_g(t) \quad I_2(t) = -I_{C2}(t) + I_g(t) \quad (13)$$

In figure 2 the waveforms of voltage and current are shown for a specific choice of the operating point,  $C$  and  $V_0$ . Since the current  $I_1$  and  $I_2$  are equal and opposite in sign, only  $I_1$  is reported. In the intervals around line current peaks the  $I_{C1}$  current has opposite sign with respect to the grid current during positive half-wave, and has the same sign during the negative half-wave. Since the current  $I_1$  flowing through the bridge is equal to the sum of the two, the peak current through the bridge is higher than the grid current peak, having a negative impact on the resulting RMS value. For example, using the same parameters as in figure 2, the RMS value of grid current is 4.35 A,  $I_{1,RMS}$  and  $I_{2,RMS}$  are 4.68 A and the RMS current

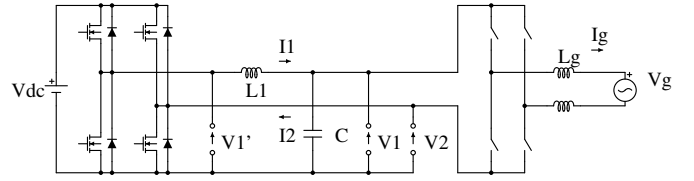


Fig. 3. Proposed topology

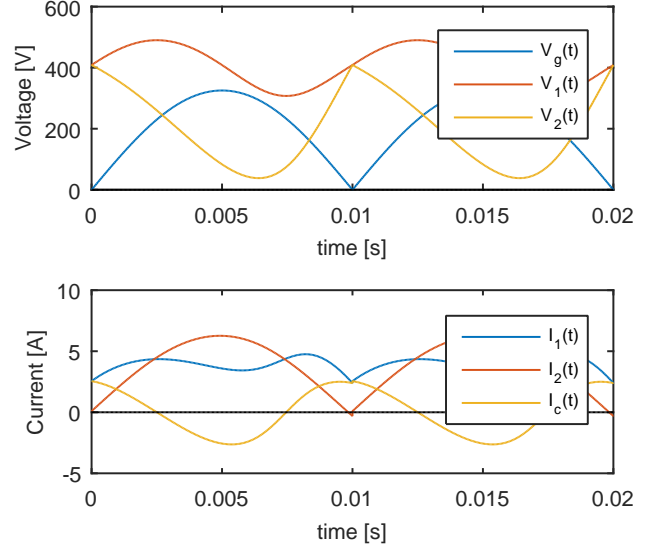


Fig. 4. Voltage and current waveforms  
 $V_{DC} = 500V, P = 1kW, C = 38\mu F$

in the capacitors are 1.74 A. Moreover, the two capacitors do not completely cooperate in providing power decoupling, since often one is charging while the other is discharging. This provides the intuition about the fact that power decoupling can be optimised by introducing suitable modifications in the topology. This leads to the new proposed topology, that uses the inherent power decoupling concepts but further reduces the capacitor needed for power decoupling.

#### IV. PROPOSED TOPOLOGY

This proposed topology is obtained by adding to the previously analysed topology a soft-switched line-commutated H-bridge switched at the zero crossings of the line voltage (ZVS) and removing one of the two capacitors, as shown in figure 3. This topology is able to provide power decoupling as the previously discussed one, while having significant advantages:

- Lower total capacitance needed;
- High efficiency of the PWM H-bridge;
- Unidirectional power flow from DC bus to grid translates in unidirectional current flow in both bridge arms (while, without line-commutated bridge, bidirectional current capability is always required).

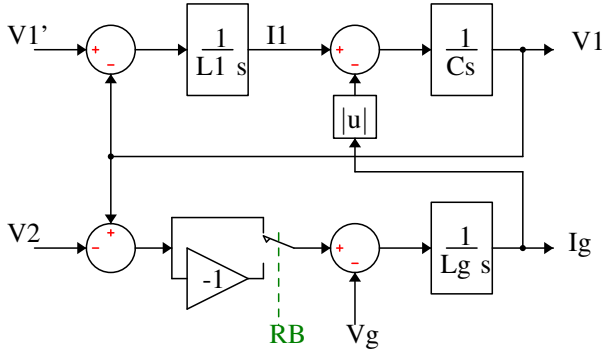


Fig. 5. Control model

Since only one capacitor is used, its voltage waveform  $V_C(t)$  can be derived directly from eq.8:

$$V_C(t) = \sqrt{\frac{P}{\omega C} \sin 2\omega t + V_0^2} \quad (14)$$

$$I_C(t) = \frac{P \cos 2\omega t}{\sqrt{\frac{P}{\omega C} \sin 2\omega t + V_0^2}} \quad (15)$$

$$V_1(t) = V_C(t) \quad V_2(t) = V_C(t) - |V_g(t)| \quad (16)$$

$$I_1(t) = |I_g(t)| + I_C(t) \quad I_2(t) = |I_g(t)| \quad (17)$$

The first harmonic component of the capacitor current is similar in magnitude to the first harmonic of rectified grid current, and almost opposite in phase. Since the high-frequency bridge arm current  $I_1$  is the sum of the two, the result is that the current waveform has an high DC component and low AC ripple, leading to lower RMS and thus better efficiency of the converter, compared to the original topology. For example, using the same parameters as in figure 4, the RMS value of grid current and  $I_{2,RMS}$  is 4.35 A,  $I_{1,RMS}$  is 3.95 A and the RMS current in the capacitor is 1.86 A. This should widely compensate the conduction losses in the line-commutated bridge. While voltage ripple in capacitors is bigger in [6], the total capacitance needed in the new topology is significantly lower.

Another advantage of this novel topology is that, as visible from the main current and voltage waveforms in fig.4, the current flowing in the PWM bridge arms is unidirectional, if unidirectional power flow is required. This is helpful because, in case of an application with unidirectional power, a diode and a switch in the high-frequency bridge are not needed, saving costs.

Since the line-commutated bridge always operates in soft-switching, switching losses are removed. For this reason, in the case in rectifier mode (power flowing only from grid to DC load), the low-frequency additional bridge can be simply made of diodes, while if the opposite power flow is required also thyristors can be used. The obvious drawbacks of this topology are conduction losses in the additional bridge and higher part counts.

## V. CONTROL CONCEPT

The proposed converter has to be able to control grid current and capacitor voltage. In order to do so, a possible control architecture is proposed. The model of the system is shown in figure 5. The control of the converter can be split, so that one PWM bridge leg can be used to control the capacitor voltage  $V_1$ , thus taking care of power ripple decoupling, while the other leg controls grid current according to the desired  $P$ , independently. This is possible because the passive net formed by inductor  $L1$ , capacitor  $C_1$  and grid inductor  $Lg$  is by all effects a LCL filter, that prevents the action of the first bridge leg to quickly affect grid current, thus effectively decoupling the control structure.

The line-commutated H-bridge does not directly interfere with current control, since it is operated at ZCS and ZVS, and the current flowing in inductor  $L_g$  is the non-rectified grid one, but the sign of voltages  $V_1$  and  $V_2$  is inverted every half-cycle. For this reason it is sufficient to change the sign of the output of the controller according to the position of the bridge. Since the steady-state waveform of the voltage  $V_2$  is known analytically (see previous section), its value is added as a *feed-forward* to the output value of the controller. The implementation of the *feed forward* of  $V_2$  is particularly helpful for the provision of the high-frequency components of its waveform.

The control structure for  $V_1$  is very simple, since it isn't affected by the line-commutated bridge. The only perturbation here is the rectified grid current, that contributes to discharge the capacitor  $C_1$ , but its high-frequency components are filtered by the large capacitance.

## VI. CAPACITOR AND $V_0$ DESIGN

The value of  $V_0$  should be calculated to provide power ripple decoupling with minimum total capacitance  $C$ . This is intuitively achieved when the voltage ripple applied to the capacitor is maximum, while respecting the constraints in terms of minimum and maximum voltage that can possibly be modulated by the PWM bridge.

The maximum ripple boundaries correspond to the voltage constraints that can be written as:

$$\max V_1(t) = V_1(t') = V_{max} \quad \min V_2(t'') = V_2(t'') = V_{min} \quad (18)$$

It can be easily seen that in case of  $V_1$  the maximum value corresponds to  $t' = \frac{\pi}{4\omega}$ , resulting in:

$$\sqrt{\frac{P}{\omega C} + V_0^2} = V_{max} \quad (19)$$

Thus:

$$V_0 = \sqrt{V_{max}^2 - \frac{P}{C}} \quad (20)$$

Finding  $t''$  is more complicated, since involves solving an equation that have no closed form solution. In order to

TABLE I  
COMPARISON CACERES-VASQUEZ [6] / PROPOSED TOPOLOGY

Vdc	P	[6] I <sub>rms</sub>	Proposed I <sub>rms</sub>	[6] C <sub>tot</sub>	Proposed C <sub>tot</sub>
[V]	[kW]	[A]	[A]	[μF]	[μF]
400	1	7.73	5.87	150	101
500	1	6.62	5.87	56	38
600	1	6.42	5.88	31	22
400	5	38.69	29.35	750	507
500	5	33.11	29.36	281	191
600	5	32.11	29.40	159	113
400	10	77.38	58.70	1500	1000
500	10	66.23	58.72	562	383
600	10	64.22	58.80	318	227

overcome this problem the minimization of  $V_2$  is approximated as the minimization of its two components, leading to:

$$\sqrt{-\frac{P}{\omega C}} + V_0^2 - \sqrt{2}V_g = V_{min} \quad (21)$$

Solving the system of eq. 20 and 21 yields the approximated values of C and  $V_0$ .

$$C = \frac{2P}{\omega} \frac{1}{V_{max}^2 - V_{min}^2 - 2V_g^2 - 2^{\frac{3}{2}}V_gV_{min}} \quad (22)$$

$$V_0 = \frac{1}{\sqrt{2}} \sqrt{V_{max}^2 + V_{min}^2 + 2V_g^2 + 2^{\frac{3}{2}}V_gV_{min}} \quad (23)$$

This approximated value of capacitance is higher than the minimum needed to respect the constraints, since the minimum value of voltage  $V_2$  calculated with this capacitance will be higher than  $V_{min}$ . This sub-optimum solution could be used when a rapid design procedure is desirable.

Instead, in order to get the correct optimum solution an iterative method can be used. Defining  $\varepsilon^k$  the difference between the calculated minimum of  $V_2^k$  and  $V_{min}$  at the step k, the problem can be iterated as following:

$$\begin{cases} \max V_1^k(t') = V_{max} \\ \min V_2^k(t'') = V_{min} - \sum_{i=1}^k \varepsilon^i \end{cases} \quad (24)$$

The iteration can be stopped when sufficiently small values of  $\varepsilon^k$  are reached.

Capacitor sizing has to be done considering the worst case scenario of maximum power transfer, since it involves the highest voltage ripple in the capacitor itself. In that case, the value of  $V_0$  is fixed by eq. 20. In case of a required power lower than the rated one,  $V_0$  can be regulated to some limits, for example, to maximize the efficiency of the converter.

A similar procedure, with some minor modifications that are omitted here, can be used for the sizing of parameters in [6].

TABLE II  
COMPARISON WITH EXISTING TOPOLOGIES

	<b>P</b>	<b>f</b>	<b>Vg</b>	<b>Vdc</b>	<b>C</b>	
	[kW]	[Hz]	[V <sub>RMS</sub> ]	[V]	[μF]	
Wang	15	233	150	540	150(200)	76
Krein	0.2	60	120	400	(3.3)	3.7
Qin	2	60	120	400	430	73

## VII. COMPARISON

Several designs were computed for different values of DC link voltage and peak power, assigning  $V_{max} = V_{DC} - 10V$  and  $V_{min} = 10V$  in order to leave a gap for control actions. The values of capacitance and  $V_0$  were then used to derive the values of RMS current in the two arms of the PWM bridge.

The values of the column  $I_{RMS}$  shown in table I are the root of sum of the squares of the calculated values of RMS current flowing through each bridge leg ( $\sqrt{I_{1RMS}^2 + I_{2RMS}^2}$ ), while the ones of the column  $C_{tot}$  are the total capacitance used. The results prove the benefits of the novel solution in terms of lower RMS current in the high-frequency bridge and minor total capacitance needed. The voltage of the grid is 230V RMS with a frequency of 50Hz.

If a certain DC link voltage is chosen, and assuming grid voltage independent from injected power, RMS currents and total capacitance grow linearly with power. In [6] a certain amount of power is circulating between the power decoupling capacitors. For this reason, since considerably higher values of capacitance are required if DC voltage is low, the total RMS current grows significantly, while in the proposed topology total RMS current is almost independent from DC voltage.

For these reasons, the proposed solution exhibits higher efficiency in the PWM bridge, at the cost of additional losses in the line-commutated one, that are anyway limited to conduction losses.

Further comparison have been made with well known power decoupling strategies, such as those described by Wang *et.al.* [2], Krein *et.al.* [3] and Qin *et.al.* [4]. The power injected in the grid and line voltage and frequency indicated in each paper were used for designing the proposed new topology, in order to compare the total capacitance.

The results are shown in table II. The first value of capacitance indicated is the one reported in the papers, and the second is the one of the proposed topology. In [2], Wang *et.al.* used a 200μF capacitor in their prototype, however the theoretical minimum capacitance needed, which is the one significant for comparison, is reported to be 150μF. In [3] the used capacitance was not explicitly indicated, but since the capacitor was fully discharged every half cycle, its value can be calculated knowing the power as 3.3μF.

The comparison shows much lower values of calculated capacitance for the proposed topology in all the cases except for the Krein topology. In [3] and [4] a high frequency full-bridge, and in [2] a half bridge, is employed, leading to higher losses according to eq.1.



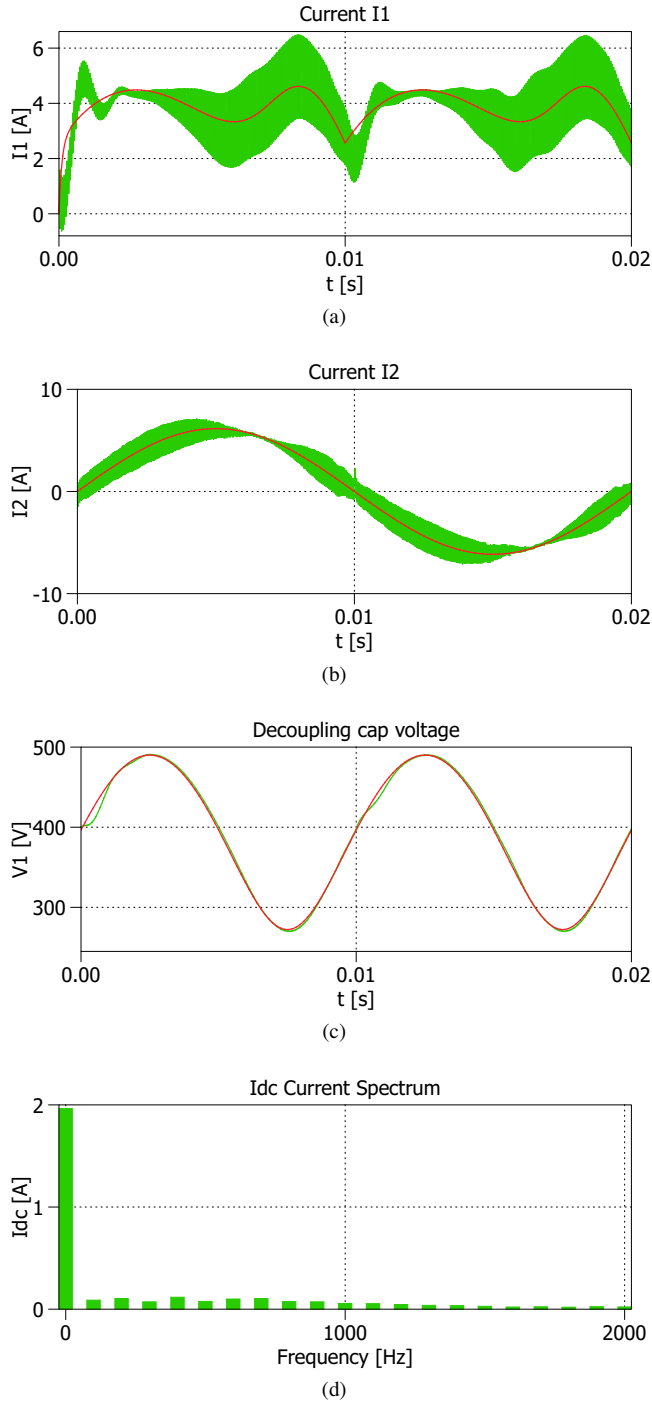


Fig. 6. Simulation results

TABLE III  
SIMULATION PARAMETERS

$V_g$	230	$V_{RMS}$	$C$	38	$\mu F$
$P$	1	kW	$V_0$	408	V
$V_{DC}$	500	V	$f_s$	20	kHz

### VIII. SIMULATION

A time domain simulation of the proposed topology was implemented using Simulink and the PLECS toolbox. Sim-

ulation parameters are shown in table III. The same values were used to plot the waveforms shown in figure 2 and 4. The resulting waveforms of current and voltage in the PWM bridge arms and DC current spectrum are shown in figure 6. The DC source was modelled as an ideal voltage source with no series impedance. The DC current spectrum confirms the correct power ripple decoupling within the converter.

### IX. CONCLUSION

This paper introduces a new AC-DC converter, suitable for low voltage distributed generation and/or energy storage systems, that provides inherent power decoupling without DC link capacitor and without a dedicated Ripple-Port. Active ripple energy storage is achieved using a line-commutated bridge operated at ZCS ZVS and a single decoupling capacitor connected on the AC side of the same PWM bridge that controls the grid current. A functional description is provided and the required total capacitance is derived analytically and compared to the capacitance of existing solutions based on concept of Ripple-Port. A simple design procedure to size the decoupling capacitor is proposed. A possible control scheme is proposed and validated in simulation. The results show that this topology offers a consistent reduction of the total capacitance needed for power ripple decoupling, making it a promising solution for developing cheap, reliable and efficient high power density single-phase converters, capable of unidirectional or bidirectional power flow.

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